REMARKS

Claims 1–20 are pending in the present application.

Claim 1 has been amended herein for explication and clarity. Claim 18 has also been amended herein.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 103 (Obviousness)

Claims 1–2, 4–5, 7, 10–12 and 14–15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over European Patent No. 0 849 684 to *Williams et al* in view of U.S. Patent No. 6,262,493 to *Garnett*. Claims 3 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Williams et al* in view of *Garnett* and further in view of U.S. Patent No. 5,754,785 to *Lysik et al*. Claims 6, 9 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Williams et al* in view of *Garnett* and further in view of European Patent No. 0 460 307 to *Gerhart et al*. Claims 8 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Williams et al* in view of *Garnett* and further in view of U.S. Patent No. 5,996,083 to *Gupta et al*. Claims 18 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Williams et al* in view of European Patent No. EP 0 898 231 to *Tavallaei* and further in view of *Garnett*. Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Williams et al* in view of *Tavallaei* and *Garnett* and further in view of *Gehart et al*. These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 3 August 2005). Absent such a *prima facie* case, the applicant is under no obligation to produce evidence of nonobviousness. *Id.*

To establish a *prima facie* case of obviousness, three basic criteria must be met: First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *Id.*

Independent claim 1 recites (a) a primary master controller inserted into the backplane and communicating with the line replaceable unit via one backplane bus when the line replaceable unit is inserted into the backplane, (b) the line replaceable unit being partially powered but lacking full access to all backplane buses and access to full power when first inserted, and (c) the primary master controller controlling full access by the line replaceable unit to the backplane buses and to full power. Similarly, independent claim 11 recites (a) inserting a primary master controller into the backplane, (b) inserting a line replaceable unit into the backplane so that the line replaceable unit is partially powered but does not have full access to all backplane buses or access to full power when

first inserted, and (c) controlling the access of the line replaceable unit to remaining buses in the backplane and full power with the primary master controller. Such a combination of features is not found in the cited references.

As conceded in the Office Action (Paper No. 20050602, page 4), *Williams et al* does not teach partially but not fully powering a line insertable unit when first inserting that line insertable unit into the backplane. The cited portion of *Garnett* states:

> When a PCI carrier connector is inserted in the power distribution connector 612, and the injector lever 542 is closed, locking the PCI carrier assembly within the chassis 200, the microswitch 540 closes, connecting the interlock signal line 536 to ground. This causes a signal to be supplied to the standby power control logic 652 and to the debounce logic 654. As soon as the microswitch 540 closes, connecting the line 536 to ground, the standby power control logic 652 is operable to provide a standby voltage from the line 662 (+5 V) via the line 626, and the line 526 to the non-volatile memory 230. Main power is not immediately connected. However, after a short time determined by the debounce logic 654 (which is powered by the main power supply VCC 660 (e.g. 14 V), a debounced interlock signal 664 is supplied to the main power control logic 650. This signal causes the main power control logic 650 to supply the main power from the supply line 660 via the main power line 622 and 522 to the DC-DC converter 524. At this time, the main circuitry of the PCI carrier assembly is powered.

Garnett, column 12, lines 19–37. Thus, *Garnett* teaches partially powering the PCI carrier until debounce logic completes a debounce, then fully powering the PCI carrier. *Garnett* does not teach that a primary master controller located on a unit inserted into another slot within the backplane controls access by the PCI carrier to full power, as recited in independent claims 1 and 11. Instead, *Garnett* teaches that the PCI carrier itself controls its own access to full power.

Independent claim 18 recites that the inserted circuit board, after being partially powered and conducting self-diagnostics such as a power on self test, connects to a common control bus to determine whether it (the inserted circuit board) should control access its own access to full power and the remaining buses or whether another circuit board should control the inserted circuit board's access to full power and other buses. In an exemplary embodiment, the inserted circuit board determines whether it has been inserted in a master controller slot, and if so whether it should configure itself as the primary master controller and either self-control access to full power and buses or as the secondary master controller subject to the primary master controllers control of access to full power and additional buses. If not inserted in a master controller slot, the inserted circuit board's access to full power and additional buses is controlled by the primary master controller. Such a feature is not found in the cited references. *Gerhart et al* is cited in the Office Action as teaching whether an inserted circuit board is inserted in a master controller slot and, if so, determining whether the inserted circuit board is a primary or secondary master controller. In fact, the cited portion of *Gerhart et al* states:

> Via these communications paths, the primary controller 30 can ensure that the secondary controller 40 is present and operational, and the secondary controller can test that the primary controller is operational to determine when it (ie., the controller designated as the secondary) is to assume the primary status (or mode).

Gerhart et al, page 4, lines 27–30. *Gerhart et al* contains no teaching regarding detecting whether an inserted circuit board was inserted into a master slot or an other slot, or determining whether an circuit board inserted into a master slot should be operated as primary or secondary master controller.

Regardless, *Gerhart et al* does not teach activating connection of a partially-powered, inserted circuit board to a common control bus to determine whether the inserted circuit board should control access to full power and other buses, or whether such control should be exercised by another inserted circuit board.

Therefore, the rejection of claims 1–20 under 35 U.S.C. § 103 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 12-9-05

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